Large-Signal HBT Model with Improved Collector Transit Time Formulation for GaAs and InP Technologies

Masaya Iwamoto, David E.Root*, Jonathan B. Scott*, Alex Cognata*,
Peter M. Asbeck, Brian Hughes*, and Don C. D'Avanzo*

Dept. of Electrical and Computer Engineering, Univ. of California at San Diego, La Jolla, CA
*Microwave Technology Center, Agilent Technologies, Santa Rosa, CA

Abstract — **An analytical large-signal HBT model which accurately accounts for the intricate bias dependence of collector delay in devices fabricated in both GaAs and InP material systems is described. The strongly bias dependent collector delay function accounts for the variation of electron velocity with electric field of the collector, which has consequences for both the electron transit time and capacitance. It is shown that the new formulation significantly improves the prediction of the bias dependence of f_t. As a result, simulations over a very wide range of operating conditions match measured data on a wide variety of devices. Distortion predictions are improved since the derivatives of the bias dependent delay are more accurately modeled. This new model is extracted on medium and high breakdown GaAs HBTs, and also on InP DHBTs. Simulation results are verified with comparisons to S-parameter and large-signal measurements.**

I. INTRODUCTION

One of the salient features of GaAs and InP-based HBTs, in contrast to Si-based bipolar transistors, is the strong bias dependence of the collector delay. The collector delay represents a significant portion of the total delay of the HBT and is clearly discernable in the f_t characteristics of the device. Recent publications on large-signal HBT models have noted the importance of proper collector delay modeling for achieving good fits to measured data [1-3]. Additionally, it has been shown that the nonlinearities due to the collector delay have a significant influence on distortion [4]. The model presented in this paper introduces an improved formulation of the collector delay function, and its proper implementation into the nonlinear circuit simulator as current- and voltage- dependent charge.

The physical concepts first articulated in [1] and implemented in the UCSD HBT model [2] were used as a starting point. A significant contribution of this work is the flexible functional forms used to represent the physical effects of collector delay and the explicit relationships derived between the small-signal bias-dependent data and the large-signal model constitutive relations.

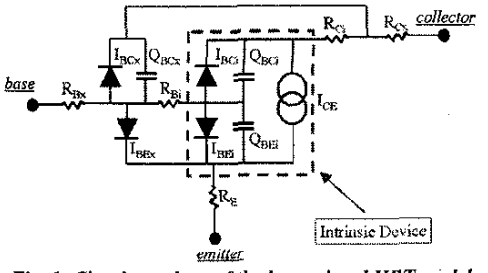

Fig. 1: Circuit topology of the large-signal HBT model

II. MODEL OVERVIEW

The lumped circuit approximation used for the model is shown in Fig. 1. The intrinsic elements are bounded within the dotted box. I_{CE} represents both the forward and reverse collector currents (I_{cf} and I_{cr}, respectively), and I_{BEi} and I_{BCi} represent the base-emitter and base-collector diodes, respectively. Q_{BEi} represents the base-emitter depletion charge and part of the diffusion (I_{cf} dependent) charge. Q_{BCi} accounts for the base-collector depletion charge and the remaining diffusion charge.

This paper will focus on the implementation of the diffusion charge of the model, which has a direct impact on the delay. Much attention will be paid to the collector delay charge, since its complex bias dependent behavior has several interesting (as well as important) consequences to the performance of the device.

III. TRANSIT TIME MODEL

Bias-dependent intrinsic delay and capacitance functions are first defined in terms of intrinsic common emitter Y-parameters. For example, the effective delay and capacitance at the input port can be defined as,

$$\tau_{in} = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega(g_m + g_{ce})} \quad (1)$$

and

$$C_{in} = \frac{\mathrm{Im}(Y_{11})}{\omega} - g_m \tau_{in} \quad (2)$$

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A model nonlinear terminal charge, representing both capacitance and transit time, can be defined by contour integration according to,

$$Q_{in}(V_{bc},I_c)=\int_{contour}[\tau_{in}(V_{bc},I_c)dI_c+C_{in}(V_{bc},I_c)dV_{bc}] \quad (3)$$

Similar expressions can be defined at the output port. A necessary and sufficient condition that must be satisfied by the data if (3) is to be unique (up to a constant) and independent of the integration path is given by,

$$\frac{\partial \tau_{in}}{\partial V_{bc}}=\frac{\partial C_{in}}{\partial I_c} \quad (4)$$

The above formulation is suitable for a measurement-based model [7], where de-embedded data can be directly substituted into (1)-(3) and nonlinear model charge functions can be calculated explicitly.

Alternatively, a flexible analytical model results if the model input terminal charge, Q_{in}, is decomposed into physically distinct current-independent depletion charges and diffusion charges which depend both on current and voltage. This is the approach taken for the model presented in this paper. The diffusion capacitance vanishes identically along any path leg defined by I_c=0, and therefore, the line integral reduces to a simple integral, with respect to I_C, of the total delay function given by,

$$Q_{in}=Q_{be}^{dep}(V_{be})+Q_{bc}^{dep}(V_{bc})+\int_0^{I_c}\tau(V_{bc},I)dI \quad (5)$$

The model current- and voltage- dependent delay, $\tau(V_{bc},I_c)$, consists of three components: base transit time (τ_B), excess delay due to Kirk effect (τ_{KE}), and collector transit time (τ_C).

τ_B describes the delay of minority carriers (i.e. electrons) traversing across the metallurgical base. For a heavily doped base, a reasonable approximation can be made in that τ_B is a constant at low and medium currents (below Kirk effect). Under this assumption, the base delay contribution to the integral in (5) is simply,

$$Q_{tB}=\tau_B \cdot I_{cf} \quad (6)$$

τ_{KE} accounts for the delay due to Kirk effect at high current injection. The formulations for the Kirk effect delay and corresponding charge functions are borrowed from the HICUM Si BJT model [5]. Since this formulation is empirical, τ_{KE} may account for other effects that may cause an increase in delay due to high current injection. A minor enhancement is made in that the critical current for Kirk effect limits at a specified V_{bc} observed in some GaAs HBT devices described by the limiting function,

$$V_{bc\_eff}=VKTR\ln\left(\exp\left(\frac{VKMX+V_{bc}}{VKTR}\right)+1\right)-VKMX \quad (7)$$

Finally, τ_C describes the bias dependence of the collector delay. The collector transit time function primarily accounts for the electric field dependence of the electron velocity. Due to the negative differential mobility characteristics of GaAs and InP, it is possible to obtain higher electron velocity (which translates to lower τ_C) at lower voltages compared to the saturated velocity at high voltages. Therefore, τ_C should decrease (from a constant saturated value) as the collector voltage is decreased. τ_C is also current dependent since electrons (negative charges) compensate the positive ionized impurity charges in the collector depletion region, altering the field profile. In general, an increase in current reduces the effective field in the collector depletion region, increasing the electron velocity [6].

The collector transit time can be approximated with 0.5(1+*tanh*) as a function of I_{cf} given by,

$$\tau_c=TCMIN\left(1-\frac{\tilde{V}_{bc}}{VTCMIN}\right)+\frac{1}{2}TFC0\left(1-\frac{\tilde{V}_{bc}}{VTC0}\right)\left(1+\tanh\left(\frac{ITC\left(1-\frac{V_{bc}}{VTC}\right)-I_{cf}}{ITC2\left(1-\frac{V_{bc}}{VTC2}\right)}\right)\right) \quad (8)$$

where $\tilde{V}_{bc}$ has a similar form as (7) to model the nonlinear dependence of electron velocity with voltage.

The simulator requires an expression for charge Q_{tc}, and so the above expression is integrated with respect to I_{Cf}. It should be reiterated that all of the delay functions τ_B, τ_{KE}, and τ_C are integrated with respect to I_{Cf} to obtain the proper contribution to the model charge function. The work in [1,2] (as well as Gummel-Poon and VBIC models), instead, formulates the model diffusion charge function as a product of the bias-dependent delay and the current. This results in a mathematical inconsistency that can result in model inaccuracies for f_t versus current and voltage, as noted in [5].

It should also be stressed that that Q_{tc} has a significant V_{BC} dependence, and so as a consequence, there is a capacitance contribution from this delay charge. Interestingly, this capacitance contribution is negative and has an effect of subtracting off the depletion capacitance, which makes the effective capacitance appear smaller (referred to as "capacitance cancellation") [6]. In general, the voltage differential of delay and the current differential of capacitance are related by the expression essentially the same as (4). This implies that the voltage dependence of transit time is intimately related to the current dependence of capacitance, and the nonlinear voltage dependence delay function has to be accurately modeled to predict the capacitance correctly. This effect is clearly evident in power devices where the charge in the lightly doped collector region is prone to modulation from both voltage and current.

Once all of the charge functions (both depletion and diffusion) are defined, they are independently partitioned to either the base-emitter or base-collector junctions.

The intrinsic base-collector charge (Q_{BCi}) is defined as,

$$Q_{BCi} = (1-ABCX)Q_{bc}^{dep} + FEXTB \cdot Q_{tB} + FEXKE \cdot Q_{KE} + FEXTC \cdot Q_{tC} \quad (11)$$

The first term accounts for the base-collector depletion charge only, and the latter terms account for the diffusion charges. ABCX is the ratio between the extrinsic base-collector area to the total base-collector area. The depletion charge function from HICUM [5] is used here since it is fully continuous for all bias conditions and accounts for the full depletion at high reverse bias. Ideally, a current dependence of Q_{bc}^{dep} is desired, since it naturally incorporates collector transit time [3]. However in the model, this current dependence is assumed to be incorporated in Q_{tc}. For the diffusion charges, the partitioning factors FEXTB, FEXKE, and FEXTC are used to account for the phase shift as transcapacitances[8].

Q_{BEi} is similarly defined as,

$$Q_{BEi} = Q_{be}^{dep} + (1-FEXTB)\cdot Q_{tB} + (1-FEXKE)\cdot Q_{KE} + (1-FEXTC)\cdot Q_{tC} \quad (12)$$

Finally, by performing KCL at the base and collector nodes, charges at the input and output for the intrinsic model are calculated,

$$Q_{in} = Q_{be}^{dep} + (1-ABCX)\cdot Q_{bc}^{dep} + Q_{tB} + Q_{tKE} + Q_{tC} \quad (13)$$

$$Q_{out} = -(1-ABCX)\cdot Q_{bc}^{dep} - FEXTB \cdot Q_{tB} - FEXKE \cdot Q_{tKE} - FEXTC \cdot Q_{tC} \quad (14)$$

By partitioning the diffusion charges in this manner, the partitioning factors only show up at the output, and all of the charges are accounted for at the input. It should be noted that (13) is the detailed model equation of (5).

IV. VALIDATION

The model was implemented as a Symbolically Defined Device (SDD) in Agilent ADS. Extractions were carried out on medium and high breakdown 2x8μm^2 emitter area InGaP/GaAs SHBTs (HBT-1 and HBT-2, respectively) and a 1x3μm^2 emitter area high speed InP DHBT (HBT-3).

HBT-1 has a BV_{CEO} of 8V. Measured f_t vs. bias characteristics are shown in Fig 2a. Fig 2b shows simulations of the extracted model over the same bias range, which closely resembles the data. As a result, S-parameter fits are accurate over a wide range of bias, as seen in Fig. 3. Since the derivatives of the bias dependant delay functions are more accurate, the model is able to predict both harmonic and intermodulation distortions accurately, as shown in Figs 4 and 5.

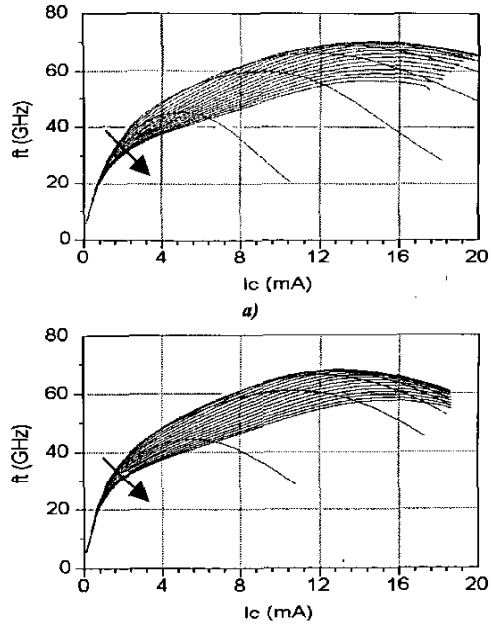

Fig 2: a) measured and b) simulated f_t vs I_C (V_{CE}=0.6 to 4V, 0.4V/step) of InGaP/GaAs HBT-1. (Arrow shows increasing V_{CE}).

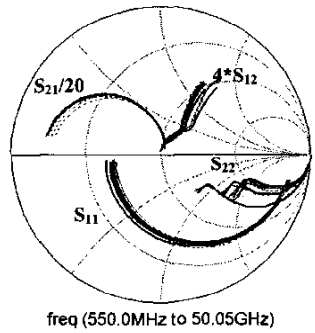

Fig 3: S-parameters from 0.55 to 50.05GHz at V_{CE}=1,2,3,4V and I_C=9.6mA of InGaP/GaAs HBT-1. (dashed=measurement, solid=simulation)

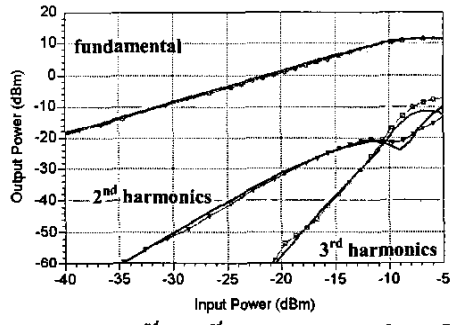

Fig 4.: Fundamental, 2nd and 3rd harmonics vs. P_{in}, freq=5GHz, R_L=264Ω, V_{CE}=3V and I_C=9.6mA of InGaP/GaAs HBT-1. (symbols=measurement, solid=simulation)

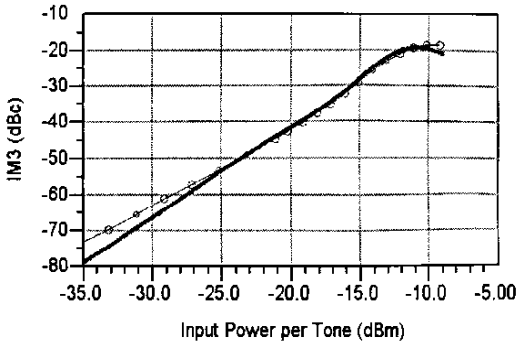

Fig 5.: IM3 vs P_{im}, freq=5GHz, Δf=1MHz, R_L=264Ω, V_{CE}=3V and I_C=9.6mA of InGaP/GaAs HBT-1. (symbols=measurement, solid=simulation)

The measured and simulated f_t vs. bias characteristics of HBT-2 (BV_{ceo}=14V) are shown in Figs 6a and b). The behavior in the medium current region before the f_t roll-off is predominantly influenced by the collector delay, and it is apparent that the model is able to account for these complex features.

Finally, Fig 7 shows measured and simulated f_t vs. bias characteristics of HBT-3. The bias dependence of f_t varies

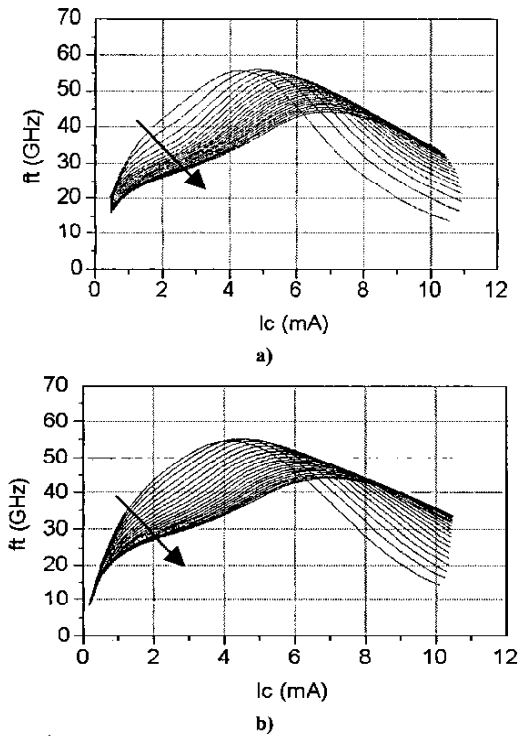

Fig 6: a) measured and b) simulated f_t vs I_C (V_{CE}=0.8 to 5V, 0.4V/step) of high breakdown InGaP/GaAs HBT-2. (Arrow shows increasing V_{CE}).

across a wide range of values, and the model demonstrates that it is able to accommodate such a device.

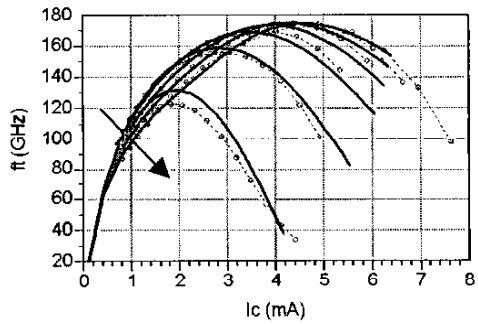

Fig 7: a) measured (dotted) and simulated (solid) f_t vs I_C (V_{CE}=0.55 to 2V, 0.29V/step) of InP DHBT HBT-3. (Arrow shows increasing V_{CE}).

V. Conclusion

A large-signal model for GaAs and InP HBTs with an improved collector transit time fromulation was presented. With the new expression for collector transit time, a better fit of f_t versus bias was achieved, which resulted in improved S-parameter and distortion simulations over a wide range of operating conditions. The model is able to accommodate various HBT devices ranging from medium (digital/mixed-signal) to high breakdown (power) processes in both GaAs and InP material systems.

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